REMARKS

Claims 1-31 are pending in the present application. Claims 1-31 are rejected. By this response, Claims 1-18, 20-23, and 25-31 continue without amendment. In view of the above the following discussion, Applicants submit that none of the claims now pending in the application are obvious under the provisions of 35 U.S.C. §103. Thus, Applicants believe that all of these claims are now in condition for allowance.

Rejection of Claims Under 35 U.S.C. §103

The Examiner rejected Claims 1-31 as being unpatentable over U.S. Publication No. 2003/0172176 granted to Fidler et al. ("Fidler") in view of U.S. Publication No. 2004/0111537 granted to Conner et al. ("Connor"). Applicants note that Claims 19 and 24 were cancelled by a previous amendment. Thus the rejection of Claims 19 and 24 is moot. The rejection of Claims 1-18, 20-23, and 25-31 is respectfully traversed.

With respect to Applicants' independent Claim 1, the Examiner stated that Fidler teaches "a transmit peripheral having a first interface configured to receive a communication sequence from a DMAC" and "a receive peripheral having a second streaming interface configured to transmit a communication sequence to the DMAC." (Final Office Action, p. 3). The Examiner cites elements in FIG. 2 of Fidler, namely, the DMA controller 18, channels 21 and 23 in the DMA controller, and the digital controller 32. The Examiner, however, did not set forth a prima facie case of obviousness.

First, the Examiner did not state how Fidler teaches or suggests a transmit peripheral and a receive peripheral. There is nothing in the Final Office Action that relates the cited DMA controller 18, channels 21 and 23, and digital controller to a transmit peripheral and a receive peripheral. The Examiner cites paragraph 0015 or Fidler, which states that data from the network is stored in a memory accessible by a processor, and data to be sent is stored in the memory prior to being read by the DMA controller. (Final Office Action, p. 3). Nothing in paragraph 0015 teaches a transmit peripheral and a receive peripheral.

Second, the Examiner did not state how Fidler teaches or suggests two streaming interfaces, one for the transmit peripheral and another for the receive peripheral. The elements 18, 21, 23, and 32 in FIG. 2 of Fidler do not include two such streaming interfaces. Applicants note that the channels 21 and 23 are both receive channels, one for broadcast data and one for non-broadcast data. (Fidler, paragraph 0014). To the extent the receive channels 21 and 23 even are streaming interfaces (which Applicants do not concede), neither of such receive channels can teach or suggest a streaming interface of a transmit peripheral.

The Examiner did not cite Connor as teaching Applicants' two streaming interfaces. Conner generally teaches a computer system that defers operating processing of previously issued operations depending on whether such operations are currently being processed. (Conner, Abstract). Conner does not teach or suggest any peripheral coupled to a streaming interface, in particular, transmit and receive peripherals each having a streaming interface. Since neither Fidler nor Conner teaches or suggests such a feature, no combination of Fidler and Conner renders obvious Applicants' invention recited in Claim 1. In addition, since the Examiner did not relate the elements of Applicants' Claim 1 to the cited references, a prima facie case of obviousness has not been established.

Independent Claim 25 recites features similar to those in Claim 1 emphasized above. Applicants contend that no combination of Fidler and Conner renders obvious Claim 25 for the same reasons discussed above.

With respect to Applicants' independent Claim 20, the Examiner stated that Fidler teaches "transmitting/receiving, over a streaming interface, [a] communication sequence to [a] DMA controller configured to control said memory circuitry." (Final Office Action, p. 5). Again, the Examiner cited elements 18, 21/23, and 32 of Fidler in FIG. 2. The Examiner also stated that Fidler teaches a "communication sequence having a header, a data section, and a footer," citing Fig. 2 of Fidler. (Final Office Action, p. 5). The Examiner, however, did not set forth a prima facie case of obviousness.

Nothing in the cited portions of Fidler teaches or suggests a communication sequence transmitted over a streaming interface to the DMA controller. The data packet (34) in Fidler is not transmitted to the DMA controller (18) over a streaming interface. Rather, the data packet (34) is a packet received from the network 12 at the physical layer 14. The MAC controller (16) in Fidler only sends the data field of the packet (34) to the DMA controller, not the entire packet (34). (See Fidler, paragraph 0020). The Examiner also cited paragraph 0018 of Fidler, which states that the RAM memory stores data carried in a single data packet 34. Applicants again note that Fidler is referring to only the data carried by the data packet, not the data packet itself.

Accordingly, Fidler does not teach or suggest transmitted the claimed communication sequence to the DMA controller. Conner is likewise devoid of any such teaching or suggestion. Thus, no conceivable combination of Fidler and Conner renders obvious Applicants' invention recited in Claim 20.

Claim 15 recites a method of communicating data between a network transceiver and memory circuitry. A communication sequence is received over a streaming interface from a DMA controller. Similar to Claim 20, the communication sequence includes a header, a data section, and a footer. As described above, the packet (34) is transmitted over the network (12) in Fidler, and is not passed to or from the DMA controller. Conner is likewise devoid of any such teaching or suggestion. Thus, no conceivable combination of Fidler and Conner renders obvious Applicants' invention recited in Claim 15.

Claims 2-14, 16-18, 20-23, and 25-31 depend from Claims 1, 15, 20, and 25 and recite additional features thereof. Since the combination of Fidler and Conner does not render obvious Applicants' invention recited in Claims 1, 15, 20, and 25, the cited combination does not render obvious Applicants' invention recited in dependent Claims 2-14, 16-18, 20-23, and 25-31.

In view of the foregoing, Applicants contend that Claims 1-18, 20-23, and 25-31 are patentable over the cited references and, as such, fully satisfy the requirements of 35 U.S.C. §103. Applicants respectfully request that the present rejection be withdrawn.

CONCLUSION

Claims 19 and 24 have been cancelled herein without prejudice. Applicants submit that none of the claims presently in the application are obvious under the provisions of 35 U.S.C. §103. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Michael R. Hardaway at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on October 22, 2007.

Julie Matthews
Name

Signature